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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER
1454.1205

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/01754	May 30, 2000	June 15, 1999

10/009979

TITLE OF INVENTION
COMPUTER-ASSISTED METHOD FOR THE PARALLEL CALCULATION OF THE OPERATING POINT OF ELECTRIC CIRCUITS

APPLICANT(S) FOR DO/EO/US
Georg DENK

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. ☒ This is an express request to immediately begin national examination procedures (35 U.S.C. 371(f)).
3. ☒ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
4. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
5. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
6. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
7. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
8. ☐ An oath or declaration of the inventor (35 U.S.C. 371(c)(4)).
9. ☒ A translation of the Annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 10-15 below concern document(s) or information included:

10. ☒ An Information Disclosure Statement Under 37 CFR 1.97 and 1.98.
11. ☐ An assignment document for recording.
    Please mail the recorded assignment document to:
    a. ☐ the person whose signature, name & address appears at the bottom of this document.
    b. ☐ the following:
12. ☒ A preliminary amendment.
13. ☒ A substitute specification
14. ☐ A change of power of attorney and/or address letter.
15. ☒ Other items or information: First page of published International Application; International Search Report; International Preliminary Examination Report.

PCT/DE00/01754

10/009979 JC07 Rec'd PCT/PTO 17 DEC 2001

The U.S. National Fee (35 U.S.C. 371(c)(1)) and other fees as follows:

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS	14 -20=	*	x $ 18.00	0.00
	INDEPENDENT CLAIMS	2 -3=	*	x $ 84.00	0.00
	MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+$280.00	0.00
	BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(4): ☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO .....$1,040 ☒ International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO.....$ 890 ☐ International preliminary examination fee (37 C.F.R. 1.482) not paid to USPTO but international search fee (37 C.F.R. 1.445(a)(2) paid to USPTO...$ 740 ☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provision of PCT Article 33(1)-(4).....$ 710 ☐ International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2) to (4) .....$ 100				890.00
	Surcharge of $130 for furnishing the National fee or oath or declaration later than ☐ 20 ☐ 30 mos. from the earliest claimed priority date (37 CFR 1.482(e)).				0.00
			TOTAL OF ABOVE CALCULATIONS		890.00
	Reduction by 1/2 for filing by small entity, if applicable. Affidavit must be filed also. (Note 37 CFR 1.9, 1.27, 1.28.)				
			SUBTOTAL		890.00
	Processing fee of $130 for furnishing the English Translation later than [ ] 20 [ ] 30 mos. from the earliest claimed priority date (37 CFR 1.482(f)).				
			TOTAL NATIONAL FEE		890.00
	Fee for recording the enclosed assignment (37 CFR 1.21(h)).				+
			TOTAL FEES ENCLOSED		890.00

a. ☐ A check in the amount of $890.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. 19-3935 in the Amount of $ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 19-3935. A duplicate copy of this sheet is enclosed.

21171
PATENT TRADEMARK OFFICE

SUBMITTED BY: STAAS & HALSEY LLP

Type Name	Mark J. Henry	Reg. No.	36,162
Signature	Mark J. Henry	Date	MJH Dec. 17, 2001

Docket No.: 1454.1205

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

PCT National Phase of PCT/DE00/01754

Georg DENK

Serial No. Group Art Unit: To be assigned

Confirmation No.

Filed: Examiner: To be assigned

For: COMPUTER-ASSISTED METHOD FOR THE PARALLEL CALCULATION OF THE OPERATING POINT OF ELECTRIC CIRCUITS

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Before examination of the above-identified application, please amend the application as follows:

IN THE ABSTRACT:

Please REPLACE the Abstract originally filed with the enclosed Substitute Abstract attached hereto.

IN THE SPECIFICATION:

Please REPLACE the specification originally filed with the enclosed Substitute Specification.

IN THE CLAIMS:

Please CANCEL claims 1-10.

Please ADD new claims 11-24 in accordance with the following:

11. (NEW) A computer-aided method for parallel calculation of the operating point of electrical circuits, comprising:

partitioning the circuit into a number of partitions in a first step; and

using the charging method for the parallel calculation of the individual partitions, a dynamic element being provided at each node of the circuit.

12. (NEW) The computer-aided method as claimed in claim 11, wherein each node of the circuit is connected to in each case a predetermined value having in each case a potential by means of in each case one capacitance so that an operating point of the modified circuit can be calculated.

13. (NEW) The computer-aided method as claimed in claim 12, wherein a capacitance having the same value is provided at each node of a partition.

14. (NEW) The computer-aided method as claimed in claim 12, wherein each node of a partition is connected to the same potential by means of a capacitance.

15. (NEW) The computer-aided method as claimed in claim 12, wherein a capacitance having the same value is provided at each node of all partitions.

16. (NEW) The computer-aided method as claimed in claim 12, wherein

each node of all partitions is connected to the same potential by means of a capacitance.

17. (NEW) The computer-aided method as claimed in claim 12, wherein the potential is connected to ground.

18. (NEW) The computer-aided method as claimed in claim 12, wherein

the operating point of the circuit is calculated in each case with a suitable step-by-step change in the value of (C) of the capacitance, and

this step is repeated until the values of the capacitances are almost zero.

19. (NEW) The computer-aided method as claimed in claim 13, wherein each node of a

partition is connected to the same potential by means of a capacitance.

20. (NEW) The computer-aided method as claimed in claim 19, wherein a capacitance having the same value is provided at each node of all partitions.

21. (NEW) The computer-aided method as claimed in claim 20, wherein

each node of all partitions is connected to the same potential by means of a capacitance.

22. (NEW) The computer-aided method as claimed in claim 21, wherein the potential is connected to ground.

23. (NEW) The computer-aided method as claimed in claim 22, wherein

the operating point of the circuit is calculated in each case with a suitable step-by-step change in the value of (C) of the capacitance, and

this step is repeated until the values of the capacitances are almost zero.

24. (NEW) A computer readable medium storing a program to control a computer to perform a method for parallel calculation of the operating point of electrical circuits, the method comprising:

partitioning the circuit into a number of partitions in a first step; and

using the charging method for the parallel calculation of the individual partitions, a dynamic element being provided at each node of the circuit.

REMARKS

This Preliminary Amendment is submitted to improve the form of the specification as originally-filed. A substitute specification and marked-up copy of the original specification are enclosed. No new matter is added to these documents.

It is respectfully requested that this Preliminary Amendment be entered in the above-referenced application.

If any further fees are required in connection with the filing of this Preliminary Amendment, please charge same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: Dec. 17, 2001

By: Mark J. Henry
Registration No. 36,162

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SUBSTITUTE ABSTRACT

A computer-aided method for parallel calculation of the operating point of electrical circuits has the circuit partitioned into a number of partitions in a first step, in which the charging method is used for the parallel calculation of the individual partitions.

SUBSTITUTE SPECIFICATION

TITLE OF THE INVENTION

COMPUTER-AIDED METHOD FOR PARALLEL CALCULATION OF THE OPERATING POINT OF ELECTRICAL CIRCUITS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is based on and hereby claims priority to German Application No. 199 27 301.4 filed on June 15, 1999 in Germany, and PCT Application No. PCT/DE00/017754 filed on May 30, 2000, the contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] The computer-aided simulation of electrical circuits has attained increasing importance in the development of very large circuits, that is to say circuits having a very large number of elements. It is particularly in the development of computer chips having a multiplicity, for example several hundred thousand transistors, that serial processing for the determination of the circuit quantities by a computer has been found to be unusable because of the excessive time consumption.

[0003] In WO 98/24039, therefore, it is proposed to partition a large circuit and to have the partitions processed by different computers in each case.

[0004] In the calculation, the operating point, that is to say the potentials of all nodes is usually determined first as basis for further analyses such as, for example, transient or alternating-current analyses.

[0005] For the parallel calculation, an implementation of the Newton method is proposed in U. Wever, Q. Zheng et al.: "Domain Decomposition Methods for Circuit Simulation" (Proceedings of the 8th Workshop on Parallel and Distributed Simulation, PADS '94 Edinburgh, Scotland, UK, pp. 183-186, July 1994) and in U. Wever, Q. Zheng: "Parallel Transient Analysis for Circuit Simulation" (Proceedings of the 29th Annual Hawaii International Conference on System Sciences, pp. 442-447, 1996). The disadvantage is that convergence can only be achieved here when sufficiently good estimates of the operating point are available, due to poor convergence characteristics. As a rule, however, such good estimates can be achieved with difficulty or not at all in the case of large circuits.

SUMMARY OF THE INVENTION

[0006] One aspect of the present invention is, therefore, based on the object of creating a computer-aided method for parallel calculation of the operating point of electrical circuits which ensures simple, reliable and fast calculation of the operating point of the circuit.

[0007] In the method, the charging method, which has very good convergence characteristics, is used for the parallel calculation of the operating point.

[0008] As described, for example, in H. Spiro: "Simulation of integrated circuits" (2nd edition, R. Oldenbourg Verlag Munich, Vienna 1990), the charging method uses the dynamic elements such as capacitances and/or inductances existing in an electrical circuit for calculating the operating point via a pseudo-transient analysis. In this process, the dynamic elements are charged up step-by-step to a value which, in principle, can have any magnitude, particularly to the value "1", starting from a value zero.

[0009] In an embodiment according to the invention, dynamic elements such as, for example, capacitances or inductances having predetermined known values can be additionally installed at suitable places, for example at or between a number of nodes. This makes it possible to avoid problems in the calculation due to the number of dynamic elements being too small.

[0010] For this purpose, the dynamic elements additionally inserted into the circuit can be reduced step-by-step to zero from an initial value, for example tending to infinity, for which the operating point calculation is trivial, so that the original circuit is again simulated.

[0011] In a preferred embodiment of the invention, at least one node, that is to say a junction of at least two current paths, of the circuit is connected by a capacitance to a predetermined value having a predetermined potential.

[0012] In a further development of the invention, however, a capacitance, the second terminal of which is in each case connected to a predetermined potential, for example to ground, can also be connected to each node via all partitions. This procedure has the advantage that the calculation of the operating point, i.e. of the respective potentials of the individual nodes, is trivial for the circuit for an initial value for the capacitances which tend toward infinity, due to the equation, which is then explicit, being solved. Changing the value for the capacitances step-by-step then makes it possible to change the circuit simulation by suitable new selection of the value for the capacitances until a calculation of the operating point of the circuit is obtained for a value of the capacitances tending toward zero or almost toward zero.

[0013] By also implementing this charging method for parallel calculation of an electrical circuit, a very large circuit having a multiplicity of transistors can be advantageously calculated in a fast and simple manner even with a smaller number of dynamic elements. Various procedures are conceivable for the respective new determination of the value for the capacitance with the aim of allowing this to go toward zero, the decision criterion being the degree of difficulty of calculating the operating point of the respective preceding step.

[0014] The operating point obtained by solving a nonlinear equation for a particular value of the capacitances in each case can be solved, for example, iteratively by the Newton method. For choosing the next value for "C", the number of iteration steps necessary for the solution can then be used until the value drops below a predetermined value for "C".

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] These and other objects and advantages of the present invention will become more apparent and more readily appreciated from the following description of the preferred embodiments, taken in conjunction with the accompanying drawings of which:

[0016] In the text which follows, the invention will be explained by means of an exemplary embodiment shown in the drawing. In the drawing, the single figure shows a flowchart which represents the individual method steps of the method.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0017] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to like elements throughout.

[0018] According to the drawing, a simulation of an electrical circuit is the starting point 1, for example in the circuit description language SPICE. This is partitioned in a first processing process 2, as described, for example, in WO 98/24039 as "Clustering method", so that individual partitions or parts of the circuits are obtained which can be calculated with the same degree of difficulty, if possible.

[0019] Naturally, other applicable variants of partitioning are conceivable such as, for example, the "ratio cut method" described in N. Fröhlich, B. Riess, U. Wever, Q. Zheng: "A new approach for parallel simulation of VLSI circuits on a transistor level" (IEEE Transaction on

Circuits and Systems – I: Fundamental Theory and Applications, Vol. 45, No. 6, June 1998, pages 601 to 613), or even an arbitrary "manual" division.

[0020] In a further process step 3, a grounded capacitance is added to each node of the circuit, that is to say to a junction of at least two conductors or current paths, respectively. Naturally, it is also conceivable to add a capacitance, the second terminal of which is connected to a predetermined potential, in which case both potentials and values for the capacitances of each node can differ. For reasons of efficiency, stability and economy of calculation, each capacitance is connected to the same potential with its second terminal, for example ground, an identically high value C0 also being selected for all capacitances in step 4 for the same reasons.

[0021] For this value C0, the operating point is then calculated for each partition or part-circuit in a further step 6, in which the required coupling values, that is to say the values for the coupling points or interfaces of adjacent partitions being exchanged and included in the calculation of the operating points of adjacent partitions.

[0022] In this process, a partition which will be called "master" in the text which follows can advantageously take over the control of the charging process for reasons of efficiency. The master then determines the initial value C0 for the capacitances, and it is also conceivable to predetermine the initial value externally, for example by the user. This value C0 is then transferred to all other partitions, called slaves in the text which follows. Following this, the operating point is calculated both in the master partition and in all slave partitions, during which process, naturally, the full source vector, which represents the energy sources existing in the circuit, is present at the circuit.

[0023] Starting from an overall problem to be solved

$$x = (m, s_1, \ldots, s_p)$$

where m is the unknowns of the master,

p is the number of partitions,

s_i is the unknowns of partition i,

the charging process leads to the system of differential equations,

$$f(x,t) + D\frac{dx}{dt} = 0$$

where

D = diag (C, ... C, 0, ..., 0) and

t is the time.

[0024] This system of differential equations can be solved, for example, by the implicit Euler method which leads to the non-linear equation

$$f(x^{k+1}, t^{k+1}) + \frac{1}{h} D(x^{k+1} - x^k) = 0$$

where x^k is the solution at time t^k for k = 0, 1, etc and h is the step $t^{k+1} - t^k$. This non-linear equation can be solved, for example, iteratively by the Newton method

$$x_{n+1}^{k+1} = x_n^{k+1} - \left(f_x\left(x_n^{k+1}, t^{k+1}\right) + \frac{1}{h} D \right)^{-1} \cdot \left(f\left(x_n^{k+1}, t^{k+1}\right) + \frac{1}{h} D\left(x_n^{k+1} - x^k\right) \right)$$

for n = 0, 1, etc.

[0025] In the parallel calculation, the master then only calculates the unknowns "m", the unknowns "s_i" representing fixed areas for the master. To be able to calculate a solution of this, the slaves or slave partitions calculate the corrected values s_i^{k+1} in each iteration step of the master and report these to the master. For this purpose, the slaves must solve the system of non-linear equations.

$$f_i\left(s_i^{k+1}, m_n^{k+1}, t^{k+1}\right) + \frac{1}{h} D_i\left(\left(s_i^{k+1}, m_i^{k+1}\right) - \left(s_i^k, m^k\right)\right) = 0$$

where f_i and D_i are the corresponding equations and matrices for the slave "i". This non-linear equation can also be calculated by the Newton method and not all iteration steps have to be necessarily performed to convergence.

[0026] The results of the slaves are then inserted into the system equations of the master whereupon the master can calculate the expression m_{n+1}^{k+1}.

[0027] In a next step 7, a new value "C_{new}" for "C" is determined by the master and the slaves can also make suggestions. To achieve the aim, namely a value for "C" tending to zero or, respectively, less than a predetermined value e, and thus a calculation of the original circuit, the

choice of the new value "C_{new}" for "C" is made dependent on the difficulty of calculating the preceding step with the value "C_{old}" for "C".

[0028] In this context, various procedures are conceivable, for example the choice of "C_{new}" in dependence on an analysis of the number of iteration steps which the master needed for calculating the non-linear system of equations for the preceding value "C_{old}" for "C":

$$C_{new} = \begin{cases} C_{old}/2 & \text{is } n < n_1 \\ C_{old} & \text{is } n_1 \leq n \leq n_2 \\ C_{old} \cdot 2 & \text{is } n_2 > n \end{cases}$$

where "n" is the number of iterations of the master and "n_1" "n_2" are the parameters predetermined by the user. Naturally, instead of halving or doubling "C_{old}", respectively, other strategies for reducing or enlarging "C_{old}" are also possible. Additionally, the number of iteration steps needed by the slaves or slave partitions for solving their non-linear system of equations can also be taken into consideration, for example through the choice of

$$n = \max\left(n, \sum_{i=1}^{n} n_i, \text{slavel}, \ldots, \sum_{i=1}^{n} n_i, \text{slavep}\right)$$

where $n_{i,\,Slavej}$ is the number of iteration steps of slave j, during the i-th iteration of the master. It must be noted in this context that the choice of a value for "C" only affects the efficiency of the method not the operating point itself.

[0029] After a value for "C" of less than or equal to a predetermined value e has been reached, the calculation is terminated at branch 5 and the value for C can be set to "0" in a last step. The operating point of the original circuit is thus found as result 8 and can be output via output units such as for example, a screen, printer or the like and/or stored in a memory as basis for further analyses of the circuit.

[0030] Due to the method described above, an operating point of a very large electrical circuit can be advantageously calculated in parallel by a multiplicity of computers or processors and the disadvantage of known parallel types of calculation, namely lack of convergence with unfavorable starting values can be avoided. Due to the parallel calculation, the expenditure for

calculation with regard to iteration steps and setting a value for "C" step by step, can be kept within tolerable limits due to the distribution to a number of processors.

[0031] The operating point thus calculated is then used as basis for further analyses, for example the alternating-current analysis of a circuit.

[0032] The invention has been described in detail with particular reference to preferred embodiments thereof and examples, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

MARKED-UP OF THE TRANSLATED INTERNATIONAL APPLICATION

[Description]TITLE OF THE INVENTION

COMPUTER-AIDED METHOD FOR PARALLEL CALCULATION OF THE OPERATING POINT OF ELECTRICAL CIRCUITS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is based on and hereby claims priority to German Application No. 199 27 301.4 filed on June 15, 1999 in Germany, and PCT Application No. PCT/DE00/017754 filed on May 30, 2000, the contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] The computer-aided simulation of electrical circuits has attained increasing importance in the development of very large circuits, that is to say circuits having a very large number of elements. It is particularly in the development of computer chips having a multiplicity, for example several hundred thousand transistors, that serial processing for the determination of the circuit quantities by a computer has been found to be unusable because of the excessive time consumption.

[0003] In WO 98/24039, therefore, it is proposed to partition a large circuit and to have the partitions processed by different computers in each case.

[0004] In the calculation, the operating point, that is to say the potentials of all nodes is usually determined first as basis for further analyses such as, for example, transient or alternating-current analyses.

[0005] For the parallel calculation, an implementation of the Newton method is proposed in U. Wever, Q. Zheng et al.: "Domain Decomposition Methods for Circuit Simulation" (Proceedings of the 8th Workshop on Parallel and Distributed Simulation, PADS '94 Edinburgh, Scotland, UK, pp. 183-186, July 1994) and in U. Wever, Q. Zheng: "Parallel Transient Analysis for Circuit Simulation" (Proceedings of the 29th Annual Hawaii International Conference on System Sciences, pp. 442-447, 1996). The disadvantage is that convergence can only be achieved here when sufficiently good estimates of the operating point are available, due to poor convergence characteristics. As a rule, however, such good estimates can be achieved with difficulty or not at all in the case of large circuits.

SUMMARY OF THE INVENTION

[0006] [The]One aspect of the present invention is, therefore, based on the object of creating a computer-aided method for parallel calculation of the operating point of electrical circuits which ensures simple, reliable and fast calculation of the operating point of the circuit. [According to the invention, this object is achieved by the method as claimed in claim 1.]

[0007] In the method, the charging method, which has very good convergence characteristics, is used for the parallel calculation of the operating point.

[0008] As described, for example, in H. Spiro: "Simulation of integrated circuits" (2nd edition, R. Oldenbourg Verlag Munich, Vienna 1990), the charging method uses the dynamic elements such as capacitances and/or inductances existing in an electrical circuit for calculating the operating point via a pseudo-transient analysis. In this process, the dynamic elements are charged up step-by-step to a value which, in principle, can have any magnitude, particularly to the value "1", starting from a value zero.

[0009] In an embodiment according to the invention, dynamic elements such as, for example, capacitances or inductances having predetermined known values can be additionally installed at suitable places, for example at or between a number of nodes. This makes it possible to avoid problems in the calculation due to the number of dynamic elements being too small.

[0010] For this purpose, the dynamic elements additionally inserted into the circuit can be reduced step-by-step to zero from an initial value, for example tending to infinity, for which the operating point calculation is trivial, so that the original circuit is again simulated.

[0011] In a preferred embodiment of the invention, at least one node, that is to say a junction of at least two current paths, of the circuit is connected by [means of] a capacitance to a predetermined value having a predetermined potential.

[0012] In a further development of the invention, however, a capacitance, the second terminal of which is in each case connected to a predetermined potential, for example to ground, can also be connected to each node via all partitions. This procedure has the advantage that the calculation of the operating point, i.e. of the respective potentials of the individual nodes, is trivial for the circuit for an initial value for the capacitances which tend toward infinity, due to the equation, which is then explicit, being solved. Changing the value for the capacitances step-by-step then makes it possible to change the circuit simulation by suitable new selection of the

value for the capacitances until a calculation of the operating point of the circuit is obtained for a value of the capacitances tending toward zero or almost toward zero.

[0013] By also implementing this charging method for parallel calculation of an electrical circuit, a very large circuit having a multiplicity of transistors can be advantageously calculated in a fast and simple manner even with a smaller number of dynamic elements. Various procedures are conceivable for the respective new determination of the value for the capacitance with the aim of allowing this to go toward zero, the decision criterion being the degree of difficulty of calculating the operating point of the respective preceding step.

[0014] The operating point obtained by solving a nonlinear equation for a particular value of the capacitances in each case can be solved, for example, iteratively by [means of] the Newton method. For choosing the next value for "C", the number of iteration steps necessary for the solution can then be used until the value drops below a predetermined value for "C". [Further advantageous embodiments of the invention are obtained from the subclaims.]

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] These and other objects and advantages of the present invention will become more apparent and more readily appreciated from the following description of the preferred embodiments, taken in conjunction with the accompanying drawings of which:

[0016] In the text which follows, the invention will be explained by means of an exemplary embodiment shown in the drawing. In the drawing, the single figure shows a flowchart which represents the individual method steps of the method.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0017] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to like elements throughout.

[0018] According to the drawing, a simulation of an electrical circuit is the starting point 1, for example in the circuit description language SPICE. This is partitioned in a first processing process 2, as described, for example, in WO 98/24039 as "Clustering method", so that individual partitions or parts of the circuits are obtained which can be calculated with the same degree of difficulty, if possible.

[0019] Naturally, other applicable variants of partitioning are conceivable such as, for example, the "ratio cut method" described in N. Fröhlich, B. Riess, U. Wever, Q. Zheng: "A new approach for parallel simulation of VLSI circuits on a transistor level" (IEEE Transaction on Circuits and Systems – I: Fundamental Theory and Applications, Vol. 45, No. 6, June 1998, pages 601 to 613), or even an arbitrary "manual" division.

[0020] In a further process step 3, a grounded capacitance is added to each node of the circuit, that is to say to a junction of at least two conductors or current paths, respectively. Naturally, it is also conceivable to add a capacitance, the second terminal of which is connected to a predetermined potential, in which case both potentials and values for the capacitances of each node can differ. For reasons of efficiency, stability and economy of calculation, each capacitance is connected to the same potential with its second terminal, for example ground, an identically high value C0 also being selected for all capacitances in step 4 for the same reasons.

[0021] For this value C0, the operating point is then calculated for each partition or part-circuit in a further step 6, in which the required coupling values, that is to say the values for the coupling points or interfaces of adjacent partitions being exchanged and included in the calculation of the operating points of adjacent partitions.

[0022] In this process, a partition which will be called "master" in the text which follows can advantageously take over the control of the charging process for reasons of efficiency. The master then determines the initial value C0 for the capacitances, and it is also conceivable to predetermine the initial value externally, for example by the user. This value C0 is then transferred to all other partitions, called slaves in the text which follows. Following this, the operating point is calculated both in the master partition and in all slave partitions, during which process, naturally, the full source vector, which represents the energy sources existing in the circuit, is present at the circuit.

[0023] Starting from an overall problem to be solved

$$x = (m, s_1, \ldots, s_p)$$

where m is the unknowns of the master,

p is the number of partitions,

s_i is the unknowns of partition i,

the charging process leads to the system of differential equations,

$$f(x,t)+D\frac{dx}{dt}=0$$

where

D = diag (C, ... C, 0, ..., 0) and

t is the time.

[0024] This system of differential equations can be solved, for example, by [means of] the implicit Euler method which leads to the non-linear equation

$$f(x^{k+1},t^{k+1})+\frac{1}{h}D(x^{k+1}-x^{k})=0$$

where x^k is the solution at time t^k for k = 0, 1, etc and h is the step $t^{k+1} - t^k$. This non-linear equation can be solved, for example, iteratively by [means of] the Newton method

$$x_{n+1}^{k+1}=x_n^{k+1}-\left(f_x\left(x_n^{k+1},t^{k+1}\right)+\frac{1}{h}D\right)^{-1}\cdot\left(f\left(x_n^{k+1},t^{k+1}\right)+\frac{1}{h}D\left(x_n^{k+1}-x^{k}\right)\right)$$

for n = 0, 1, etc.

[0025] In the parallel calculation, the master then only calculates the unknowns "m", the unknowns "s_i" representing fixed areas for the master. To be able to calculate a solution of this, the slaves or slave partitions calculate the corrected values s_i^{k+1} in each iteration step of the master and report these to the master. For this purpose, the slaves must solve the system of non-linear equations.

$$f_i\left(s_i^{k+1},m_n^{k+1},t^{k+1}\right)+\frac{1}{h}D_i\left(\left(s_i^{k+1},m_i^{k+1}\right)-\left(s_i^{k},m^{k}\right)\right)=0$$

where f_i and D_i are the corresponding equations and matrices for the slave "i". This non-linear equation can also be calculated by [means of] the Newton method and not all iteration steps have to be necessarily performed to convergence.

[0026] The results of the slaves are then inserted into the system equations of the master whereupon the master can calculate the expression m_{n+1}^{k+1}.

[0027] In a next step 7, a new value "C_{new}" for "C" is determined by the master and the slaves can also make suggestions. To achieve the aim, namely a value for "C" tending to zero or, respectively, less than a predetermined value e, and thus a calculation of the original circuit, the choice of the new value "C_{new}" for "C" is made dependent on the difficulty of calculating the preceding step with the value "C_{old}" for "C".

[0028] In this context, various procedures are conceivable, for example the choice of "C_{new}" in dependence on an analysis of the number of iteration steps which the master needed for calculating the non-linear system of equations for the preceding value "C_{old}" for "C":

$$C_{new} = \begin{cases} C_{old}/2 & \text{is } n < n_1 \\ C_{old} & \text{is } n_1 \le n \le n_2 \\ C_{old} \cdot 2 & \text{is } n_2 > n \end{cases}$$

where "n" is the number of iterations of the master and "n_1" "n_2" are the parameters predetermined by the user. Naturally, instead of halving or doubling "C_{old}", respectively, other strategies for reducing or enlarging "C_{old}" are also possible. Additionally, the number of iteration steps needed by the slaves or slave partitions for solving their non-linear system of equations can also be taken into consideration, for example through the choice of

$$n = \max\left(n, \sum_{i=1}^{n} n_i, \text{slavel}, \ldots, \sum_{i=1}^{n} n_i, \text{slavep} \right)$$

where $n_{i,\,Slavej}$ is the number of iteration steps of slave j, during the i-th iteration of the master. It must be noted in this context that the choice of a value for "C" only affects the efficiency of the method not the operating point itself.

[0029] After a value for "C" of less than or equal to a predetermined value e has been reached, the calculation is terminated at branch 5 and the value for C can be set to "0" in a last step. The operating point of the original circuit is thus found as result 8 and can be output via output units such as for example, a screen, printer or the like and/or stored in a memory as basis for further analyses of the circuit.

[0030] Due to the method [according to the invention]described above, an operating point of a very large electrical circuit can be advantageously calculated in parallel by a multiplicity of computers or processors and the disadvantage of known parallel types of calculation, namely lack of convergence with unfavorable starting values can be avoided. Due to the parallel calculation, the expenditure for calculation with regard to iteration steps and setting a value for "C" step by step, can be kept within tolerable limits due to the distribution to a number of processors.

[0031] The operating point thus calculated is then used as basis for further analyses, for example the alternating-current analysis of a circuit.

[0032] The invention has been described in detail with particular reference to preferred embodiments thereof and examples, but it will be understood that variations and modifications can be effected within the spirit and scope of the invention.

Description

Computer-aided method for parallel calculation of the operating point of electrical circuits

The computer-aided simulation of electrical circuits has attained increasing importance in the development of very large circuits, that is to say circuits having a very large number of elements. It is particularly in the development of computer chips having a multiplicity, for example several hundred thousand transistors, that serial processing for the determination of the circuit quantities by a computer has been found to be unusable because of the excessive time consumption.

In WO 98/24039, therefore, it is proposed to partition a large circuit and to have the partitions processed by different computers in each case.

In the calculation, the operating point, that is to say the potentials of all nodes is usually determined first as basis for further analyses such as, for example, transient or alternating-current analyses.

For the parallel calculation, an implementation of the Newton method is proposed in U. Wever, Q. Zheng et al.: "Domain Decomposition Methods for Circuit Simulation" (Proceedings of the 8th Workshop on Parallel and Distributed Simulation, PADS '94 Edinburgh, Scotland, UK, pp. 183-186, July 1994) and in U. Wever, Q. Zheng: "Parallel Transient Analysis for Circuit Simulation" (Proceedings of the 29th Annual Hawaii International Conference on System Sciences, pp. 442-447, 1996). The disadvantage is that convergence can only be achieved here when sufficiently good estimates of the operating point are available, due to poor convergence characteristics. As a rule, however, such good

estimates can be achieved with difficulty or not at all in the case of large circuits.

The present invention is, therefore, based on the object of creating a computer-aided method for parallel calculation of the operating point of electrical circuits which ensures simple, reliable and fast calculation of the operating point of the circuit.

According to the invention, this object is achieved by the method as claimed in claim 1.

In the method, the charging method, which has very good convergence characteristics, is used for the parallel calculation of the operating point.

As described, for example, in H. Spiro: "Simulation of integrated circuits" (2nd edition, R. Oldenbourg Verlag Munich, Vienna 1990), the charging method uses the dynamic elements such as capacitances and/or inductances existing in an electrical circuit for calculating the operating point via a pseudo-transient analysis. In this process, the dynamic elements are charged up step-by-step to a value which, in principle, can have any magnitude, particularly to the value "1", starting from a value zero.

In an embodiment according to the invention, dynamic elements such as, for example, capacitances or inductances having predetermined known values can be additionally installed at suitable places, for example at or between a number of nodes. This makes it possible to avoid problems in the calculation due to the number of dynamic elements being too small.

For this purpose, the dynamic elements additionally inserted into the circuit can be reduced step-by-step to zero from an initial value, for example tending to infinity, for which the operating point calculation is trivial, so that the original circuit is again simulated.

In a preferred embodiment of the invention, at least one node, that is to say a junction of at least two current paths, of the circuit is connected by means of a capacitance to a predetermined value having a predetermined potential.

In a further development of the invention, however, a capacitance, the second terminal of which is in each case connected to a predetermined potential, for example to ground, can also be connected to each node via all partitions. This procedure has the advantage that the calculation of the operating point, i.e. of the respective potentials of the individual nodes, is trivial for the circuit for an initial value for the capacitances which tend toward infinity, due to the equation, which is then explicit, being solved. Changing the value for the capacitances step-by-step then makes it possible to change the circuit simulation by suitable new selection of the value for the capacitances until a calculation of the operating point of the circuit is obtained for a value of the capacitances tending toward zero or almost toward zero.

By also implementing this charging method for parallel calculation of an electrical circuit, a very large circuit having a multiplicity of transistors can be advantageously calculated in a fast and simple manner even with a smaller number of dynamic elements. Various procedures are conceivable for the respective new determination of the value for the capacitance with the aim of allowing this to go toward zero, the decision criterion being the degree of difficulty of calculating the operating point of the respective preceding step.

The operating point obtained by solving a nonlinear equation for a particular value of the capacitances in each case can be solved, for example, iteratively by means of the Newton method. For choosing the next value for "C",

the number of iteration steps necessary for the solution can then be used until the value drops below a predetermined value for "C".

Further advantageous embodiments of the invention are obtained from the subclaims.

In the text which follows, the invention will be explained by means of an exemplary embodiment shown in the drawing. In the drawing, the single figure shows a flowchart which represents the individual method steps of the method.

According to the drawing, a simulation of an electrical circuit is the starting point 1, for example in the circuit description language SPICE. This is partitioned in a first processing process 2, as described, for example, in WO 98/24039 as "Clustering method", so that individual partitions or parts of the circuits are obtained which can be calculated with the same degree of difficulty, if possible.

Naturally, other applicable variants of partitioning are conceivable such as, for example, the "ratio cut method" described in N. Fröhlich, B. Riess, U. Wever, Q. Zheng: "A new approach for parallel simulation of VLSI circuits on a transistor level" (IEEE Transaction on Circuits and Systems - I: Fundamental Theory and Applications, Vol. 45, No. 6, June 1998, pages 601 to 613), or even an arbitrary "manual" division.

In a further process step 3, a grounded capacitance is added to each node of the circuit, that is to say to a junction of at least two conductors or current paths, respectively. Naturally, it is also conceivable to add a capacitance, the second terminal of which is connected to a predetermined potential, in which case both potentials and values for the capacitances of each node

can differ. For reasons of efficiency, stability and economy of calculation, each capacitance is connected to the same potential with its second terminal, for example ground, an identically high value C0 also being selected for all capacitances in step 4 for the same reasons.

For this value C0, the operating point is then calculated for each partition or part-circuit in a further step 6, in which the required coupling values, that is to say the values for the coupling points or interfaces of adjacent partitions being exchanged and included in the calculation of the operating points of adjacent partitions.

In this process, a partition which will be called "master" in the text which follows can advantageously take over the control of the charging process for reasons of efficiency. The master then determines the initial value C0 for the capacitances, and it is also conceivable to predetermine the initial value externally, for example by the user. This value C0 is then transferred to all other partitions, called slaves in the text which follows. Following this, the operating point is calculated both in the master partition and in all slave partitions, during which process, naturally, the full source vector, which represents the energy sources existing in the circuit, is present at the circuit.

Starting from an overall problem to be solved

$$x = (m, s_1, \ldots, s_p)$$

where m is the unknowns of the master,

p is the number of partitions,

s_i is the unknowns of partition i,

the charging process leads to the system of differential equations,

$$f(x,t)+D\frac{dx}{dt}=0$$

where

D = diag (C, ... C, 0, ..., 0) and
t is the time.

This system of differential equations can be solved, for example, by means of the implicit Euler method which leads to the non-linear equation

$$f(x^{k+1},t^{k+1})+\frac{1}{h}D(x^{k+1}-x^{k})=0$$

where x^k is the solution at time t^k for k = 0, 1, etc and h is the step $t^{k+1} - t^k$. This non-linear equation can be solved, for example, iteratively by means of the Newton method

$$x_{n+1}^{k+1}=x_{n}^{k+1}-\left(f_x\left(x_n^{k+1},t^{k+1}\right)+\frac{1}{h}D\right)^{-1}\cdot\left(f\left(x_n^{k+1},t^{k+1}\right)+\frac{1}{h}D\left(x_n^{k+1}-x^{k}\right)\right)$$

for n = 0, 1, etc.

In the parallel calculation, the master then only calculates the unknowns "m", the unknowns "s_i" representing fixed areas for the master. To be able to calculate a solution of this, the slaves or slave partitions calculate the corrected values s_i^{k+1} in each iteration step of the master and report these to the master. For this purpose, the slaves must solve the system of non-linear equations.

$$f_i\left(s_i^{k+1}, m_n^{k+1}, t^{k+1}\right) + \frac{1}{h} D_i\left(\left(s_i^{k+1}, m_i^{k+1}\right) - \left(s_i^k, m^k\right)\right) = 0$$

where f_i and D_i are the corresponding equations and matrices for the slave "i". This non-linear equation can also be calculated by means of the Newton method and not all iteration steps have to be necessarily performed to convergence.

The results of the slaves are then inserted into the system equations of the master whereupon the master can calculate the expression m_{n+1}^{k+1}.

In a next step 7, a new value "C_{new}" for "C" is determined by the master and the slaves can also make suggestions. To achieve the aim, namely a value for "C" tending to zero or, respectively, less than a predetermined value e, and thus a calculation of the original circuit, the choice of the new value "C_{new}" for "C" is made dependent on the difficulty of calculating the preceding step with the value "C_{old}" for "C".

In this context, various procedures are conceivable, for example the choice of "C_{new}" in dependence on an analysis of the number of iteration steps which the master needed for calculating the non-linear system of equations for the preceding value "C_{old}" for "C":

$$C_{new} = \begin{cases} C_{old}/2 & \text{is } n < n_1 \\ C_{old} & \text{is } n_1 \le n \le n_2 \\ C_{old} \cdot 2 & \text{is } n_2 > n \end{cases}$$

where "n" is the number of iterations of the master and "n_1" "n_2" are the parameters predetermined by the user. Naturally, instead of halving or doubling "C_{old}", respectively, other strategies for reducing or enlarging "C_{old}" are also possible. Additionally, the number of iteration steps needed by the slaves or slave partitions for solving their non-linear system of equations can also be taken into consideration, for example through the choice of

$$n = \max\left(n, \sum_{i=1}^{n} n_i, \text{slavel}, \ldots, \sum_{i=1}^{n} n_i, \text{slavep}\right)$$

where $n_{i,\ slavej}$ is the number of iteration steps of slave j, during the i-th iteration of the master. It must be noted in this context that the choice of a value for "C" only affects the efficiency of the method not the operating point itself.

After a value for "C" of less than or equal to a predetermined value e has been reached, the calculation is terminated at branch 5 and the value for C can be set to "0" in a last step. The operating point of the original circuit is thus found as result 8 and can be output via output units such as for example, a screen, printer or the like and/or stored in a memory as basis for further analyses of the circuit.

Due to the method according to the invention, an operating point of a very large electrical circuit can be advantageously calculated in parallel by a multiplicity of computers or processors and the disadvantage of known parallel types of calculation, namely lack of convergence with unfavorable starting values can be avoided. Due to the parallel calculation, the expenditure for calculation with regard to iteration steps and

setting a value for "C" step by step, can be kept within tolerable limits due to the distribution to a number of processors.

The operating point thus calculated is then used as basis for further analyses, for example the alternating-current analysis of a circuit.

Patent claims

1. A computer-aided method for parallel calculation of the operating point of electrical circuits,
   - in which the circuit is partitioned into a number of partitions in a first step,

   characterized in that
   - the charging method is used for the parallel calculation of the individual partitions.

2. The computer-aided method as claimed in claim 1, characterized in that a dynamic element (C, L) is provided and at least one node of the circuit.

3. The computer-aided method as claimed in claim 2, characterized in that a dynamic element (C, L) is provided at each node of the circuit.

4. The computer-aided method as claimed in claim 2 or 3, characterized in that each node of the circuit is connected by means of in each case one capacitance to in each case a predetermined value having in each case a potential so that an operating point of the modified circuit can be calculated.

5. The computer-aided method as claimed in claim 4, characterized in that a capacitance having the same value (C0) is provided at each node of a partition.

6. The computer-aided method as claimed in claim 4 or 5, characterized in that each node of a partition is connected to the same potential by means of a capacitance.

7. The computer-aided method as claimed in claim 4, characterized in that a capacitance having the same value (C0) is provided at each node of all partitions.

8. The computer-aided method as claimed in claim 4 or 7, characterized in that each node of all partitions is connected to the same potential by means of a capacitance.

9. The computer-aided method as claimed in one of claims 4 to 7, characterized in that the potential is connected to ground.

10. The computer-aided method as claimed in one of claims 4 to 8, characterized in that

- the operating point of the circuit is calculated in each case with a suitable step-by-step change in the value of (C) of the capacitance, and
- this step is repeated until the values of the capacitances are almost zero.

11. A computer program product which can be loaded into a main memory of a computer system, with a software code for carrying out the method according to one of the preceding claims when the computer program product is running on a computer system.

12. A data carrier with a computer program product as claimed in claim 11.

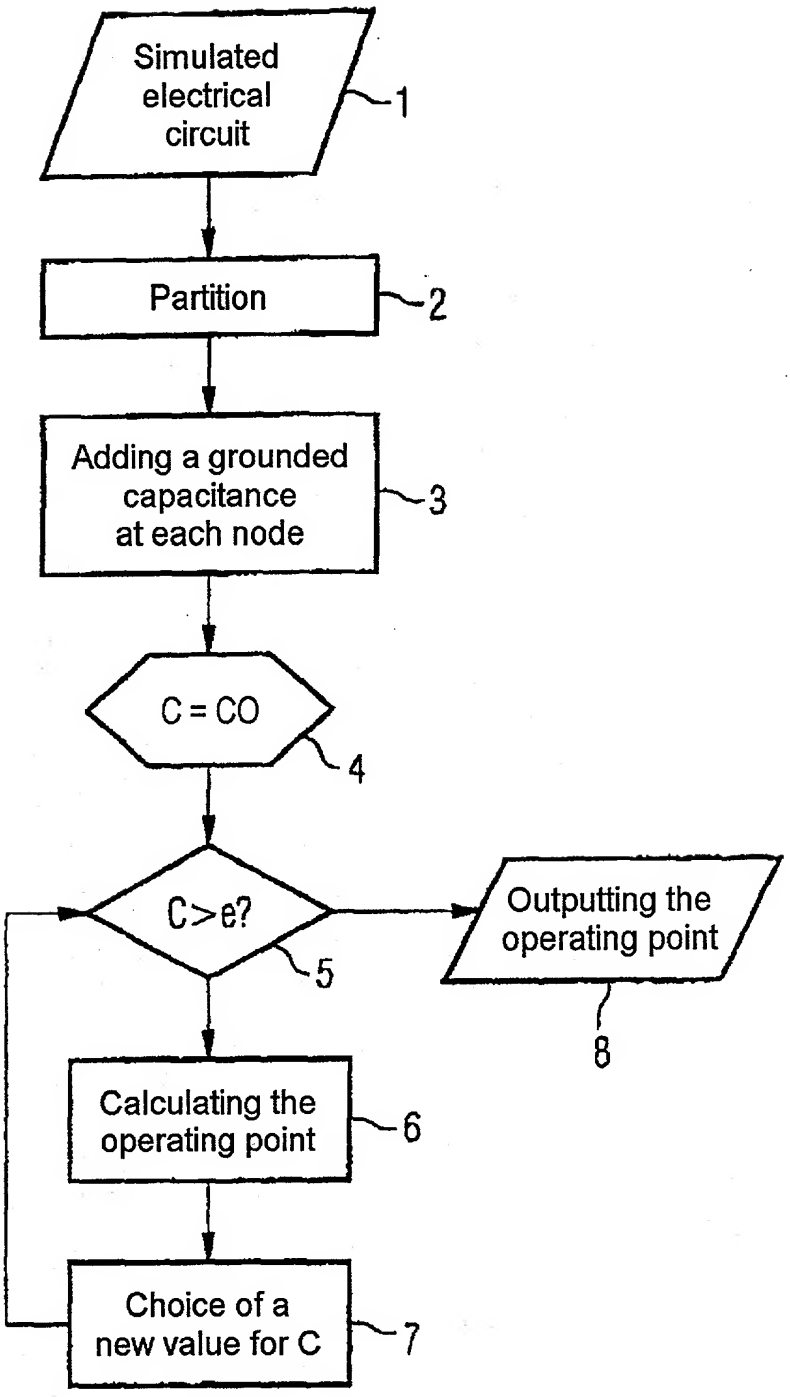
GR 99 P 2008

Abstract

Computer-aided method for parallel calculation of the operating point of electrical circuits

The invention relates to a computer-aided method for parallel calculation of the operating point of electrical circuits, in which the circuit is partitioned into a number of partitions in a first step, in which the charging method is used for the parallel calculation of the individual partitions.

The single figure is the main drawing.



Patent claims

1. A computer-aided method for parallel calculation of the operating point of electrical circuits,
   - in which the circuit is partitioned into a number of partitions in a first step,

   characterized in that
   - the charging method is used for the parallel calculation of the individual partitions, a dynamic element (C, L) being provided at each node of the circuit.

2. The computer-aided method as claimed in claim 1, characterized in that each node of the circuit is connected to in each case a predetermined value having in each case a potential by means of in each case one capacitance so that an operating point of the modified circuit can be calculated.

3. The computer-aided method as claimed in claim 2, characterized in that a capacitance having the same value (C0) is provided at each node of a partition.

4. The computer-aided method as claimed in claim 2 or 3, characterized in that each node of a partition is connected to the same potential by means of a capacitance.

5. The computer-aided method as claimed in claim 2, characterized in that a capacitance having the same value (C0) is provided at each node of all partitions.

6. The computer-aided method as claimed in claim 2 or 5, characterized in that

each node of all partitions is connected to the same potential by means of a capacitance.

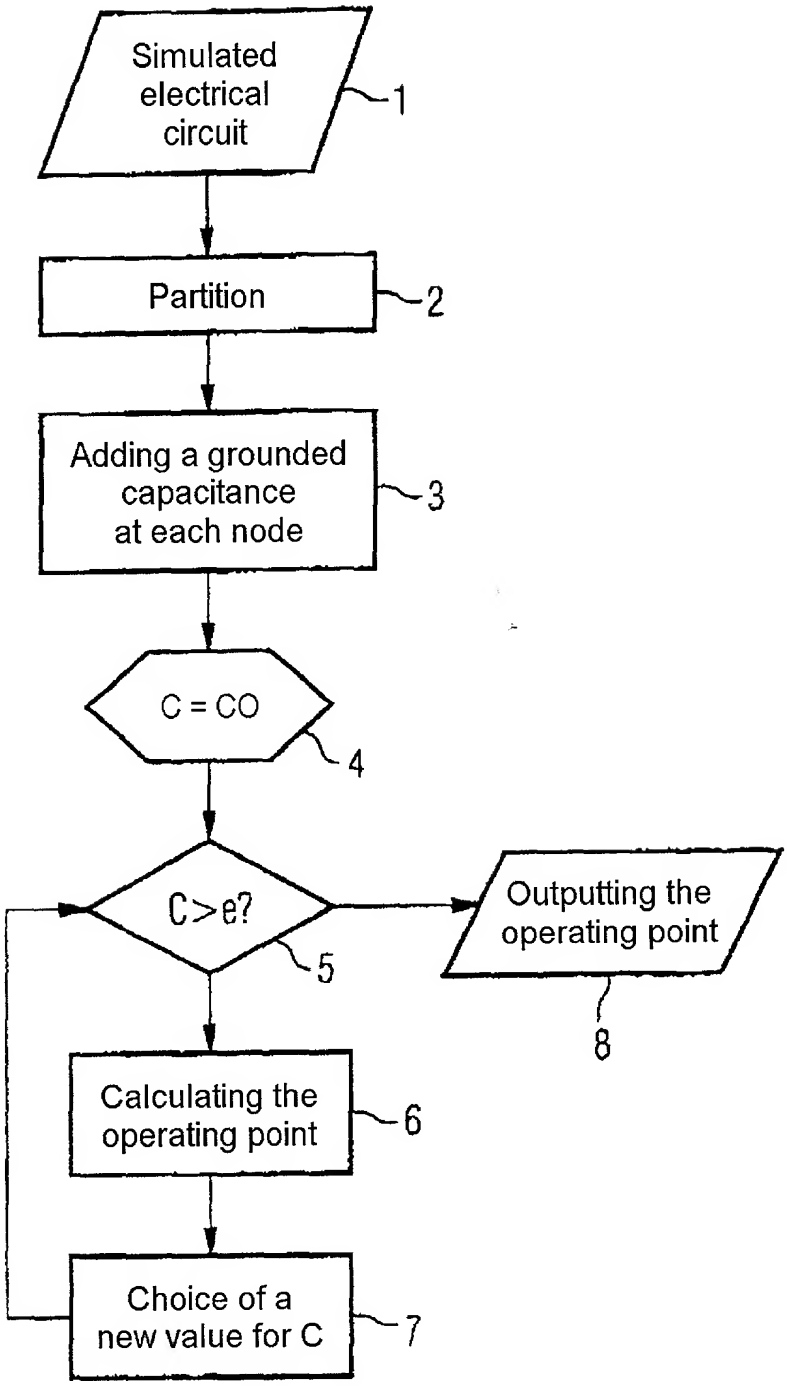
7. The computer-aided method as claimed in one of claims 2 to 5, characterized in that the potential is connected to ground.

8. The computer-aided method as claimed in one of claims 2 to 6, characterized in that

- the operating point of the circuit is calculated in each case with a suitable step-by-step change in the value of (C) of the capacitance, and
- this step is repeated until the values of the capacitances are almost zero.

9. A computer program product which can be loaded into a main memory of a computer system, with a software code for carrying out the method according to one of the preceding claims when the computer program product is running on a computer system.

10. A data carrier with a computer program product as claimed in claim 9.



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I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Rechnergestütztes Verfahren zur parallelen Berechnung des Arbeitspunktes elektrischer Schaltungen

Computer-assisted method for the parallel calculation of the operating point of electric circuits

deren Beschreibung

the specification of which

(zutreffendes ankreuzen)
☐ hier beigefügt ist.
☒ am 30.05.2000 als
PCT internationale Anmeldung
PCT Anmeldungsnummer PCT/DE00/01754
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Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

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I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

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Prior foreign appplications
Priorität beansprucht

			Priority Claimed	
19927301.4	DE	15.06.1999	☒	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein
			☐	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein
			☐	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

PCT/DE00/01754 (Application Serial No.) (Anmeldeseriennummer)	30.05.2000 (Filing Date D, M, Y) (Anmeldedatum T, M, J)	anhängig (Status) (patentiert, anhängig, aufgegeben)	pending (Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date D,M,Y) (Anmeldedatum T, M; J)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

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German Language Declaration

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Dr. GEORG DENK	Dr. GEORG DENK
Unterschrift des Erfinders Datum	Inventor's signature Date
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Wohnsitz	Residence
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83026 ROSENHEIM	83026 ROSENHEIM
Voller Name des zweiten Miterfinders (falls zutreffend):	Full name of second joint inventor, if any:
Unterschrift des Erfinders Datum	Second Inventor's signature Date
Wohnsitz	Residence
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(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors).